AMENDMENTS TO THE CLAIMS

Please add new claims 58-99.

LISTING OF CLAIMS

Claims 1-39: (Cancelled.)

40.(Previously Presented) A nonvolatile memory system comprising:

a nonvolatile memory including a plurality of nonvolatile memory cells and a shift register; and

a control device coupled to said nonvolatile memory, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memory,

wherein said nonvolatile memory is enabled to operate a program operation,

wherein in said program operation, said nonvolatile memory receives said data from said control device, stores said data to said shift register and stores said data in said shift register to ones of said nonvolatile memory cells,

wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memory is operating in said program operation, and

wherein said shift register has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.

Claims 41-46: (Cancelled.)

47.(Previously Presented) A nonvolatile memory system according to claim 40,

wherein said nonvolatile memory includes a plurality of word lines and a plurality of data lines, and wherein each of said nonvolatile memory cells is arranged at a crossing point of a corresponding one of said word lines and a corresponding one of said data lines and is coupled to the corresponding word line and corresponding data line.

48.(Previously Presented) A nonvolatile memory system according to claim 47,

wherein said nonvolatile memory includes a plurality of sectors each comprising one word line and ones of the nonvolatile memory cells coupled thereto, and wherein said shift register has a data storing capacity enabling the receiving of a unit of data of a length equal to the data storing capacity and enabling the storing of a unit of data in said sector.

49.(Previously Presented) A nonvolatile memory system according to claim 48, wherein said nonvolatile memory is a flash memory.

50.(Previously Presented) A nonvolatile memory system according to claim 40,

wherein said control device includes a host interface comprised of a data bus transceiver, an address bus driver, an address decoder and a control bus controller, to enable communication between the nonvolatile memory and an external system bus.

51.(Previously Presented) A nonvolatile memory system comprising:

a plurality of nonvolatile memories each including a plurality of nonvolatile memory cells and a shift register; and

a control device coupled to said nonvolatile memories, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memories,

wherein said nonvolatile memories are enabled to operate a program operation,

wherein in said program operation, each of said nonvolatile memories selectively receives said data from said control device, stores said data to said shift register thereof and stores said data in said shift register to ones of said nonvolatile memory cells of that nonvolatile memory,

wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memories are operating in said program operation, and

wherein said shift register has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.

Claim 52: (Cancelled.)

53.(Previously Presented) A nonvolatile memory system according to claim 51,

wherein each of said nonvolatile memories further includes a plurality of word lines and a plurality of data lines, and

wherein each of said nonvolatile memory cells in each of the nonvolatile memories is arranged at a crossing point of a corresponding one of said word lines and a corresponding one of said data lines and is coupled to said corresponding word line and corresponding data line.

54.(Previously Presented) A nonvolatile memory system according to claim 53,

wherein each of said nonvolatile memories includes a plurality of sectors each comprising one word line and ones of the nonvolatile memory cells coupled thereto, and

wherein said shift register has a data storing capacity for receiving data in units of a sector and enabling the storing of a unit of data in said sector.

55.(Previously Presented) A nonvolatile memory system accordance to claim 54,

wherein each of said nonvolatile memories is a flash memory.

56.(Previously Presented) A nonvolatile memory system according to claim 55,

wherein said control device includes a host interface comprised of a data bus transceiver, an address bus driver, an address decoder and a control bus controller, to enable communication between the nonvolatile memories and an external system bus.

57.(Previously Presented) A nonvolatile memory system according to claim 51,

wherein said control device includes a host interface comprised of a data bus transceiver, an address bus driver, an address decoder and a control bus controller, to enable communication between the nonvolatile memories and an external system bus.

58.(New) The non-volatile memory system of claim 40, wherein said non-volatile memory receives said data from said control device serially.

59.(New) The non-volatile memory system of claim 58, wherein said non-volatile memory receives said data from said control device serially in a multi-bit manner.

60.(New) The non-volatile memory system of claim 58, wherein said control device receive data from outside of said nonvolatile memory system serially and accumulate the data in the control device prior to sending the data to the non-volatile memory.

61.(New) The non-volatile memory system of claim 60, where data is transferred in parallel on the control device.

62.(New) The non-volatile memory system of claim 40, wherein the control device includes error correction circuitry whereby corresponding error correction code is generated for data received from outside of said nonvolatile memory device.

63.(New) The non-volatile memory system of claim 62, wherein subsequent to said nonvolatile memory receiving said data from said control device, said nonvolatile memory receives the corresponding error correction code for said data from said control devices.

64.(New) The non-volatile memory system of claim 51, wherein said non-volatile memory receives said data from said control device serially.

65.(New) The non-volatile memory system of claim 64, wherein said non-volatile memory receives said data from said control device serially in a multi-bit manner.

66.(New) The non-volatile memory system of claim 64, wherein said control device receive data from outside of said nonvolatile memory system serially and accumulate the data in the control device prior to sending the data to the non-volatile memory.

67.(New) The non-volatile memory system of claim 66, where data is transferred in parallel on the control device.

68.(New) The non-volatile memory system of claim 51, wherein the control device includes error correction circuitry whereby corresponding error correction code is generated for data received from outside of said nonvolatile memory device.

69.(New) The non-volatile memory system of claim 68, wherein subsequent to said nonvolatile memory receiving said data from said control device, said nonvolatile memory receives the corresponding error correction code for said data from said control devices.

70.(New) The nonvolatile memory system of claim 51, wherein prior to said nonvolatile memories selectively receiving said data from said control device, the nonvolatile memories receive a device specific address whereby a selected nonvolatile memory is specified.

71.(New) The nonvolatile memory system of claim 70, wherein each of the nonvolatile memories has a device specific logical state set on one or more pins and a nonvolatile memory device is selected by comparing the device specific address to the nonvolatile memory's corresponding logical state set on the pins.

72.(New) A method of operating a nonvolatile memory system, the memory system including a controller and a first memory coupled to the controller, the first memory having a non-volatile memory array and a register having a capacity able to store a unit of data equivalent to the length of data to be stored at one time in a program operation, said data length being more than one byte, the method comprising:

receiving data from outside of the nonvolatile memory system at the controller;

subsequently transferring the data from the controller to the first memory;

storing the data received from the controller in the register of the first memory; and

thereafter writing the data from the register to non-volatile memory array of the first memory.

73.(New) The method of claim 72, wherein the transferring of the data from the controller to the first memory is a serial transfer of data.

74.(New) The method of claim 73, wherein the serial transfer of data is a multi-bit serial transfer.

75.(New) The method of claim 73, wherein the controller receives the data from outside of the nonvolatile memory system serially and the method further includes:

accumulating the data in the controller prior to transferring the data to the first memory.

76.(New) The method of claim 75, the method further including:

after accumulating the data in the controller prior to transferring the data to the first memory, transferring the data in parallel on the controller.

77.(New) The method of claim 72, wherein the controller includes error correction circuitry, the method further comprising:

generating corresponding error correction code for the data received from outside of said nonvolatile memory system.

78.(New) The method of claim 77, further comprising:

subsequent to transferring the data from the controller to the first memory, transferring the corresponding error correction code for the data from the controller to the first memory.

79.(New) The method of claim 72, wherein the non-volatile memory system includes a plurality of memories coupled to the controller each having a non-volatile memory array and a register having a capacity able to store a unit of data equivalent to the length of data to be stored at one time in a program operation, the method further including:

selecting the first memory from the plurality of memories prior to transferring the data from the controller to the first memory.

80.(New) The method of claim 79, wherein selecting the first memory device includes:

sending a device specific address to the memory devices whereby the first memory is specified.

81.(New) The method of claim 80, wherein each of the memories has a device specific logical state set on one or more pins and selecting the first memory device further includes:

comparing the device specific address to the first memory's corresponding logical state set on the pins.

82.(New) A method of operating a nonvolatile memory system including a plurality of memories each having a non-volatile memory array and a register having a capacity able to store a unit of data equivalent to the length of data to be stored at one time in a program operation, said data length being more than one byte, each of the memories having a plurality of pins with a device specific logical state on one or more of the corresponding pins, the method comprising:

receiving at the memories an address;

performing on the memories a comparison of a portion of the received address with the device specific logical states;

selecting a first of the memories based upon the comparisons;

subsequent to receiving at each of the memories the address, receiving data at the memories;

storing the received data in the register of the first memory; and

thereafter writing the data from the register to non-volatile memory array of the first memory.

83.(New) The method of claim 82, wherein the address and the data are received serially.

84.(New) The method of claim 83, wherein the address and the data are received as a multi-bit serial transfer.

85.(New) The method of claim 82, further comprising:

subsequent to receiving the data at the memories, receiving error correction code corresponding to the data at the memories.

86.(New) The method of claim 82, wherein the memory system further includes a controller coupled to the plurality of memories, the method further comprising:

prior to receiving data at the memories, receiving said data from outside of the nonvolatile memory system at the controller; and

subsequently transferring the data from the controller to the memories.

87.(New) The method of claim 86, wherein the transferring of the data from the controller to the memories is a serial transfer of data.

88.(New) The method of claim 87, wherein the serial transfer of data is a multi-bit serial transfer.

89.(New) The method of claim 86, wherein the controller receives the data from outside of the nonvolatile memory system serially and the method further includes:

accumulating the data in the controller prior to transferring the data to the memories.

90.(New) The method of claim 89, the method further including:

after accumulating the data in the controller prior to transferring the data to the memories, transferring the data in parallel on the controller.

91.(New) The method of claim 86, wherein the controller includes error correction circuitry, the method further comprising:

generating corresponding error correction code for the data received from outside of said nonvolatile memory system.

92.(New) The method of claim 91, further comprising:

subsequent to transferring the data from the controller to the memories, transferring the corresponding error correction code for the data from the controller to the memories.

93.(New) A nonvolatile memory system comprising:

a plurality of memories, each having:

a non-volatile memory array;

a register having a capacity able to store a unit of data equivalent to the length of data to be stored at one time in a program operation;

programming circuitry connectable to the array and the register to write data content from the register to the array;

device select circuitry; and

a plurality of pins connectable to the device select circuitry with a device specific logical state on one or more of the pins; and

a control module coupled to said nonvolatile memories, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memories,

wherein, in a program operation, the control module transfers an address to the memories and subsequently transfers data to the memories, and the memories compare in the device select circuitry a portion of the received address with the device specific logical states and a first of the memories is selected based upon the comparisons, the data being stored in the register of the first memory and subsequently written into the array of the first memory.

94.(New) The nonvolatile memory system of claim 93, wherein the address and the data are transferred serially.

95.(New) The nonvolatile memory system of claim 94, wherein the address and the data are received as a multi-bit serial transfer.

96.(New) The nonvolatile memory system of claim 93, wherein the control module receives the data from outside of the nonvolatile memory system serially and accumulates the data in the control module prior to transferring the data to the memories.

97.(New) The nonvolatile memory system of claim 96, wherein after accumulating the data in the control module prior to transferring the data to the memories, the data is transferred in parallel on the control module.

98.(New) The nonvolatile memory system of claim 93, wherein the control module further includes error correction circuitry to generate corresponding error correction code for the data received from outside of said nonvolatile memory system.

99.(New) The nonvolatile memory system of claim 98, wherein subsequent to transferring the data from the control module to the memories, the corresponding error correction code for the data is transferred from the controller to the memories.